

**AMENDMENTS TO THE SPECIFICATIONS:**

**Please replace paragraph [0001] with the following amended paragraph:**

**[0001]** This application claims priority to U.S. Provisional Application Serial No. 60/400,391 titled "JSM Protection," filed July 31, 2002, incorporated herein by reference. This application also claims priority to EPO Application No. 03291927.6, filed July 30, 2003 and entitled "A Multi-Processor Computing System Having A Java Stack Machine And A RISC-Based Processor," incorporated herein by reference. This application also may contain subject matter that may relate to the following commonly assigned co-pending applications incorporated herein by reference: "System And Method To Automatically Stack And Unstack Java Local Variables," Serial No. 10/632,228, filed July 31, 2003, Attorney Docket No. TI-35422 (1962-05401); "Memory Management Of Local Variables," Serial No. 10/632,067, filed July 31, 2003, Attorney Docket No. TI-35423 (1962-05402); "Memory Management Of Local Variables Upon A Change Of Context," Serial No. 10/632,076, filed July 31, 2003, Attorney Docket No. TI-35424 (1962-05403); "A Processor With A Split Stack," Serial No. 10/632,079, filed July 31, 2003, Attorney Docket No. TI-35425(1962-05404); "Using IMPDEP2 For System Commands Related To Java Accelerator Hardware," Serial No. 10/632,069, filed July 31, 2003, Attorney Docket No. TI-35426 (1962-05405); "Test With Immediate And Skip Processor Instruction," Serial No. 10/632,214, filed July 31, 2003, Attorney Docket No. TI-35427 (1962-05406); "Test And Skip Processor Instruction Having At Least One Register Operand," Serial No. 10/632,084, filed July 31, 2003, Attorney Docket No. TI-35248 (1962-05407); "Synchronizing Stack Storage," Serial No. 10/631,422, filed July 31, 2003, Attorney Docket No. TI-35429 (1962-05408); "Methods And Apparatuses For Managing Memory," Serial No. 10/631,252, filed July 31, 2003, Attorney Docket No. TI-35430 (1962-05409); "Write Back Policy For Memory," Serial No. 10/631,185, filed July 31, 2003, Attorney Docket No. TI-35431 (1962-05410); "Methods And Apparatuses For Managing Memory," Serial No. 10/631,205, filed July 31, 2003, Attorney Docket No. TI-35432 (1962-05411); "Mixed Stack-Based RISC Processor," Serial No. 10/631,308, filed July 31, 2003, Attorney Docket No. TI-35433 (1962-05412); "Processor That Accommodates Multiple Instruction Sets And Multiple Decode Modes," Serial No. 10/631,246, filed July 31, 2003, Attorney Docket No. TI-35434 (1962-05413); "System To Dispatch Several Instructions On Available Hardware Resources," Serial No. 10/631,585, filed July 31, 2003,

**Appl. No. 10/632,077**  
**Amdt. dated August 6, 2007**  
**Reply to Office Action of April 4, 2007**

Attorney Docket No. TI-35444 (1962-05414); “Micro-Sequence Execution In A Processor,” Serial No. 10/632,216, filed July 31, 2003, Attorney Docket No. TI-35445 (1962-05415); “Program Counter Adjustment Based On The Detection Of An Instruction Prefix,” Serial No. 10/632,222, filed July 31, 2003, Attorney Docket No. TI-35452 (1962-05416); “Reformat Logic To Translate Between A Virtual Address And A Compressed Physical Address,” Serial No. 10/632,215, filed July 31, 2003, Attorney Docket No. TI-35460 (1962-05417); “Synchronization Of Processor States,” Serial No. 10/632,024, filed July 31, 2003, Attorney Docket No. TI-35461 (1962-05418); “Conditional Garbage Based On Monitoring To Improve Real Time Performance,” Serial No. 10/631,195, filed July 31, 2003, Attorney Docket No. TI-35485 (1962-05419); “Inter-Processor Control,” Serial No. 10/631,120, filed July 31, 2003, Attorney Docket No. TI-35486 (1962-05420); “Cache Coherency In A Multi-Processor System,” Serial No. 10/632,229, filed July 31, 2003, Attorney Docket No. TI-35637 (1962-05421); and “Concurrent Task Execution In A Multi-Processor, Single Operating System Environment,” Serial No. 10/632,077, filed July 31, 2003, Attorney Docket No. TI-35638 (1962-05422).

**Please replace paragraph [0032] with the following amended paragraph:**

[0032] After finishing the task prompted by the system interrupt 209, the MPU 104 may read the status of the JSM 102. If the JSM 102 is in an idle state (i.e., the JSM 102 is not actively executing instructions), the MPU 104 may execute one or more instructions ~~one or more~~ on behalf of the JSM 102. As previously described, the JSM 102 may encounter an instruction that requires, or at least benefits from, the support of the MPU 104. Thus, this instruction may be executed by the MPU 104.

**Please replace paragraph [0042] with the following amended paragraph:**

[0042] System 100 may be representative of, or adapted to, a wide variety of electronic systems, an exemplary electronic system may comprise a battery-operated, mobile cell phone such as that shown in Figure 6. As shown in Figure 6, a mobile communications device 415 includes an integrated keypad 412 and display 414. The JSM 102 and MPU 104 noted above and other components may be included in electronics package 410 which may be coupled to keypad ~~410~~ 415, display 414, and radio frequency (“RF”) circuitry 416 which may be connected to an antenna 418.